CLAIMS IN CURRENT FORM

1. (ORIGINAL) An apparatus comprising:

an analog circuit configured to generate a plurality of samples of an input signal in response to a plurality of phases of a reference clock; and

a digital circuit configured to (i) measure a width of a symbol in said input signal in response to said plurality of samples and said plurality of phases of said reference clock and (ii) adjust said measured width in response to a correction signal.

2. (ORIGINAL) The apparatus according to claim 1, wherein said digital circuit comprises a width counter circuit configured to measure said width of said symbol.

3. (ORIGINAL) The apparatus according to claim 2, wherein said width counter circuit is configured to measure said width of said symbol in response to a number of edges of a predetermined one of said plurality of phases that occur between a first edge and a second edge of said input signal.

4. (ORIGINAL) The apparatus according to claim 1, wherein said digital circuit is configured to generate a scratch signal in response to said measured width being larger than a predetermined value.

5. (ORIGINAL) The apparatus according to claim 1, wherein said digital circuit is configured to determine whether said measured symbol width represents a logic HIGH symbol or a logic LOW symbol.

6. (ORIGINAL) The apparatus according to claim 5, wherein said correction signal comprises a HIGH data correction signal and a LOW data correction signal.

7. (ORIGINAL) The apparatus according to claim 1, wherein said correction signal is generated in response to a number of width measurements.

8. (ORIGINAL) The apparatus according to claim 1, wherein said digital circuit is configured to generate said correction signal when in a locked state.

9. (ORIGINAL) The apparatus according to claim 8, wherein said digital circuit is configured to maintain said locked state during detection of a scratch.

10. (ORIGINAL) The apparatus according to claim 1, wherein said correction signal is configured to compensate for a rise time of said input signal.

11. (ORIGINAL) The apparatus according to claim 1, wherein said correction signal is configured to compensate for a fall time of said input signal.

12. (ORIGINAL) An apparatus comprising:

means for generating a plurality of samples of an input signal in response to a plurality of phases of a reference clock; and

means for measuring a width of a symbol in said input signal in response to said plurality of samples and said plurality of phases of said reference clock; and

means for adjusting said measured width in response to a correction signal.

13. (PREVIOUSLY PRESENTED) A method for correcting a measured width of a symbol in an input signal comprising the steps of:

(A) generating a plurality of samples of said input signal in response to a plurality of phases of a reference clock;

(B) measuring said width of said symbol in said input signal in response to said plurality of samples and said plurality of phases of said reference clock; and

(C) adjusting said measured width in response to a correction signal.

14. (ORIGINAL) The method according to claim 13, wherein step (B) further comprises the sub-step of:

detecting an edge of said symbol in said input signal.

15. (ORIGINAL) The method according to claim 14, wherein step (B) further comprises the sub-step of:

determining a position of said edge with respect to said plurality of phases.

16. (ORIGINAL) The method according to claim 15, wherein step (B) further comprises the sub-step of:

calculating a current symbol length of said input signal.

17. (ORIGINAL) The method according to claim 16, further comprising the step of:

generating a scratch signal in response to a symbol length greater than a predetermined value.

18. (ORIGINAL) The method according to claim 16, wherein step (C) further comprises the sub-step of:

adjusting said current symbol length in response to said correction signal and a portion of a previous symbol length.

19. (PREVIOUSLY PRESENTED) The method according to claim 13, further comprising the step of:

generating a calculated bit width based on a plurality of adjusted symbol lengths.

20. (ORIGINAL) The method according to claim 19, further comprising the step of:

generating an output signal in response to said input signal and said calculated bit width.